Remarks

Examiner Natneal is thanked for the helpful telephone conference of September 13, 2004. In response to the interview and the Office Action mailed July 9, 2004, claims 1, 4-5, 10-11, 13 and 15-16 are herein amended. New claims 17-18 that contain subject matter similar to claims 13 and 14, are herein presented. Claims 1-18 are now pending in the application. No new matter has been entered.

The instant invention relates to a system for reducing clock jitter while transmitting video data through a plurality of serially connected video stages. In order to accomplish a reduction of clock jitter, each stage within the present system contains a digital video scaler (DVS), a constant frequency clock and a multiplexer. Each and every stage of the present system subjects the input video signal from the previous stage to the DVS for scaling to a constant resolution using the constant frequency clock. In the present invention, the DVS contained in each stage provides an asynchronous boundary between the incoming video stream which may contain a jittery clock signal and the output video signal which is clocked using the constant frequency clock. In this manner the video signal integrity is maintained by reclocking within every stage.

Claims 1-16 have been rejected in view of the MacInnis (6,738,072) patent in view of the Admitted Prior Art (APA) as described in the application. In the rejection of the above claims, the Office Action relies on the combination of the DVS contained in Figure 5 of MacInnis as modified by the APA. As discussed in the interview and summarized below, Applicants respectfully disagree with the Office Action's treatment of two specifically claimed features of the invention. These two claimed features are the "constant frequency clock" and the "DVS" contained in each stage of the present system.

Regarding the claimed feature of the constant frequency clock, the Office Action asserts that "a constant frequency clock connected to the DVS (contained in MacInnis) is implied because without a clock or timing signal the scaler 52 may not be synchronized properly". Applicants respectfully disagree with this statement, as systems commonly have multiple clocks with different frequencies as evidenced by the Admitted Prior Art. In the APA each individual stage has a programmable clock that may be set to any desired frequency. Therefore the claimed feature of a constant frequency clock is not inherent in MacInnis and would certainly not be obvious in view of the teachings of the Admitted Prior Art, which explicitly teaches away from employing constant frequency clocks.

Regarding the claimed feature of the DVS scaling the video data to a constant resolution in each stage of the present system, the Office Action asserts that "Although a preceding stage and/or next stage are not specified in the MacInnis et al reference, it would be obvious to those with ordinary skill in the art that the preceding stage would be the video source or head-end and the next stage would be the television set itself". "Therefore, it would have been obvious to modify the system of MacInnis by providing the prior art system of Figures 1 and 2 of the APA in order to better synchronize the transmission of video signal from one stage (head-end) to the receiver or television set so that flicker or flutter is minimized".

Again as discussed in the interview, Applicants respectfully submit that it is not obvious to employ a DVS in each and every stage of a daisy chain of connected stages. As conventional displays are capable of displaying video data regardless of transmitted resolution, it would not be necessary (nor obvious) to provide a DVS in each stage. Further, once video data has been scaled to a predetermined constant resolution, there is no reason to scale the data again to the same constant resolution. Essentially the DVS in each stage is not being used for its known purpose (scaling), but to provide a data reclocking function. Therefore it would not have been obvious to one of ordinary skill in the art to modify MacInnis with a DVS in every stage.

Regarding the Examiner's objection to claims 4-5, 10-11 and 15-16, the terms "LVDS" and "TMDS" are now defined in the claims as supported on page 4 of the instant specification.

Applicant respectfully submits that in light of the amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned Agent if any issues remain.

Respectfully submitted,
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Date: December 9, 2004

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